Orbis™
BiSS C Register Access

Abstract: The BiSS-C interface implemented in Orbis supports bidirectional communication in register access mode. The readhead is user programmable and includes 4 kB of user memory. The implementation is compliant with the BiSS Standard Encoder Profile (also called as “BP3”), which is used for grouping linear and rotary encoders. Details on BiSS register access and BP3 can be found in the **iC-Haus documentation**.

User implementation: The user can implement bidirectional BiSS in their own hardware according to the BiSS documentation provided by iC-Haus. The user can also use the iC-Haus chip iC-MB4, which translates the high-level commands on the SPI bus into BiSS. The easiest way is to use the interface E201-9B from RLS including the corresponding software.

Related products

Orbis true absolute rotary encoder

E201-9B USB interface

Registers description

BiSS memory map for Orbis

Bank	Address	Data type	Access	Description
0	0x00 – 0x03	U32	R/W	Position offset
	0x04 – 0x07	U32	R/W	Multiturn counter preset
	0x08 – 0x2D	U8	R	Reserved
	0x2E	U8	R/W	Write protect lock
	0x2F – 0x30	U16	R	FW major version
	0x31 – 0x32	U16	R	FW minor version
	0x33 – 0x34	U16	R	Protocol version
	0x35 – 0x36	U16	R	Revision number
	0x3F	U8	R	Checksum of bank 0
1 - 15	0x00 – 0x3F	U8	R	Reserved
16	0x00 – 0x3F	U8	R	BiSS EDS common part
17	0x00 – 0x3F	U8	R	BiSS EDS standard encoder profile
18 - 23	0x00 – 0x3F	U8	R	Reserved
24 - 87	0x00 – 0x3F	U8	R/W	User memory
Direct access	0x40	U8	R/W	Bank select
	0x41	U8	R	EDS bank
	0x42 – 0x43	U16	R	Profile ID
	0x44 – 0x47	U32	R	Serial number
	0x48	U8	R/W	Key register
	0x49	U8	R/W	Command register
	0x4A – 0x4B	U16	R	Encoder status (table A)
	0x4C – 0x4D	U16	R	Temperature (K)
	0x50	U8	R	Self-calibration status
	0x51-0x52	U16	R	Signal level
	0x53	U8	R	Multiturn status (0)
	0x54-0x5B	U8	R	Reserved
	0x5C – 0x61	U8	R	RLS serial number
	0x62 – 0x63	U8	R	Reserved
	0x64 – 0x73	U8	R	RLS part number
	0x74 – 0x77	U8	R	Reserved
	0x78 – 0x7D	U48	R	Device ID
	0x7E – 0x7F	U16	R	Manufacturer ID

U16, U32, U48 data is saved as a Big Endian (highest-value byte at the lowest-value address).

BiSS EDS common part

Address	Symbol	Description	Data type	Unit	Value
0x00	EDS_VER	EDS version	U8	-	1
0x01	EDS_LEN	EDS length	U8	banks	2
0x02	USR_STA	Bank address USER start	U8	-	24
0x03	USR_END	Bank address USER end	U8	-	87
0x04	TMA	Min. permitted clock period	U8	1 ns	200
0x05	TO_MIN	Min. BiSS timeout	U8	250 ns	52
0x06	TO_MAX	Max. BiSS timeout	U8	250 ns	60
0x07	TOS_MIN	Min. BiSS timeout_S	U8	25 ns	0
0x08	TOS_MAX	Max. BiSS timeout_S	U8	25 ns	0
0x09	TCLK_MIN	Min. sampling period adaptive timeout	U8	25 ns	0
0x0A	TCLK_MAX	Max. sampling period adaptive timeout	U8	25 ns	0
0x0B	TCYC	Min. cycle time	U8	250 ns	100
0x0C	TBUSY_S	Max. processing time SCD	U8	250 ns	0
0x0D	BUSY_S	Max. processing time SCD in clocks	U8	TMA	5
0x0E – 0x0F	PON_DLY	Max. “power on delay” until control communication is available	U16	1 ms	100
0x10	DC_NUM	Number of data channel in this device	U8	-	1
0x11	SL_NUM	Area of validity for this EDS (number of slave addresses)	U8	-	1
0x12	SL_OFF	Memory location for this EDS (slave ID within this device)	U8	-	0
0x13		Reserved	U8		0
0x14	BANK1	Bank address for content description of data channel 1 (Profile EDS)	U8	-	17
0x15	DLEN1	Data length for data channel 1	U8	bit	table B
0x16	FORMAT1	Data format for data channel 1	U8	bit	2
0x17	CPOLY1	CRC polynomial (8:1) for data channel 1	U8	-	0x21
0x18 – 0x33		Reserved	U8		0
0x34	BC_OFF	Bus coupler control location for this device (slave ID within this device)	U8	-	0
0x35 – 0x3E		Reserved	U8		0
0x3F	CHKSUM	Checksum (sum of all bytes within this bank)	U8	-	xx

U16 data is saved as a Big Endian (highest-value byte at the lowest-value address).

Table A

Encoder status:
0x4A:
b7: System error
b6: System error
b5: Angle comparison error
b4: Safety comparison error
b3: Reserved
b2: Reserved
b1: Global error. If high, the position data is not valid.
b0: Global warning. If high, the position is valid, but some operating conditions are close to limits.

0x4B:
b7: Signal amplitude too high. The readhead is too close to the magnet or an external magnetic field is present.
b6: Signal amplitude low. The distance between the readhead and the ring is too large.
b5: The readhead temperature is out of specified range.
b4: Speed too high.
b3: Multiturn error/warning (optionally)
b2: Reserved
b1: Reserved
b0: Reserved

Table B

	Encoder type	
EDS parameter	14 bit Singleturn	14 bit Multiturn
DLEN1	16	32

BiSS EDS standard encoder profile

Address	Symbol	Description	Data type	Unit	Value
0x00	BP_VER	BiSS profile 3 version	U8	-	1
0x01	BP_LEN	Length of this profile	U8	banks	1
0x02 – 0x03	BP_ID	Profile identification BP3 (content also available in addresses 0x42 and 0x43)	U16	-	table C
0x04	FB1	Feedback bit 1 (nError = 1)	U8	-	1
0x05	FB2	Feedback bit 2 (nWarning = 2)	U8	-	2
0x06	PON_PDL	Max. “power on delay” until position data is available	U8	ms	100
0x07		Reserved	U8	-	0
0x08	EN_TYP	Encoder type (rotary = 0)	U8	-	0
0x09	POS_NUM	Position value (1 position)	U8	-	1
0x0A	MT_LEN	Data length MULTITURN	U8	bit	table C
0x0B	MT_FMT	Data format MULTITURN	U8	-	table C
0x0C	CO_LEN	Data length COARSE	U8	bit	0
0x0D	CO_FMT	Data format COARSE	U8	-	0
0x0E	FI_LEN	Data length FINE	U8	bit	table C
0x0F	FI_FMT	Data format FINE	U8	-	0
0x10 – 0x13	MT_CNT	Number of distinguishable revolutions	U32	count	table C
0x14 – 0x17	SIP_CNT	Number of signal periods per revolution	U32	PPR	1
0x18 – 0x1B	SIP_RES	Resolution factor per signal period (LSB of interpolation)	U32	count	table C
0x1C – 0x1F	CPOLY	CRC polynomial (32:1 of 0x43)	U32	-	0x21
0x20 – 0x23	CSTART	CRC start value	U32	-	0
0x24 – 0x25	ABS_ACU	Absolute accuracy	U16	LSB/2	18
0x26 – 0x27	REL_ACU	Relative accuracy	U16	LSB/2	0
0x28 – 0x29	SPD_ACU	Angular speed depending accuracy	U16	LSB/2	0
0x2A – 0x2B	HYST	Hysteresis	U16	LSB/2	0
0x2C – 0x2D	SPD_MAX	Max. revolution speed	U16	1/min	10000
0x2E – 0x2F	ACC_MAX	Max. revolution acceleration	U16	1/min2	0
0x30 – 0x31	TMP_MIN	Min. operating temperature	U16	K	273
0x32 – 0x33	TMP_MAX	Max. operating temperature	U16	K	358 (378)
0x34 – 0x35	VLT_MIN	Min. operating voltage	U16	mV	4500
0x36 – 0x37	VLT_MAX	Max. operating voltage	U16	mV	5500
0x38 – 0x39	CUR_MAX	Max. current consumption	U16	mA	70
0x3A – 0x3E		Reserved	U8		0
0x3F	CHKSUM	Checksum (sum of all bytes within this bank)	U8	-	xx

U16, U32 data is saved as a Big Endian (highest-value byte at the lowest-value address).

Table C

Encoder type	EDS BP3 parameter					
	BP_ID	MT_LEN	MT_FMT	FI_LEN	MT_CNT	SIP_RES
14 bit ST	0x6210	0	0	14	0	16384
14 bit MT	0x6220	16	1	14	65536	16384

ST - Singleturn
MT - Multiturn

Bank switching

BiSS registers are grouped into banks of 64 bytes. Each register in each bank can be accessed with an address from 0x00 to 0x3F. Before you can access a particular bank, it must be selected in the Bank select register, which maps to address 0x40. If the bank number written to register 0x40 exceeds the maximum available bank number (87), the bank number is reset to its default value (0). For more information on bank switching, refer to the documentation provided by iC-Haus.

Read access

All registers in Orbis memory can be read. Read access also supports sequential reading. It is possible to read up to 64 bytes forward from the initialized read address. A detailed description of the sequential read access can be found in the iC-Haus documentation.

Write access

The writeable registers in the Orbis memory are listed in the “Memory map” table. All registers can be write-protected if user write access is disabled, except for the Bank select register. Sequential write access is only available in User memory banks, otherwise it is denied. For a detailed description of sequential write access, refer to the iC-Haus documentation.

Orbis programming

The orbis readhead can be programmed with a position offset (zero position of the encoder), a multiturn counter (optional) and a register write protection. In addition, the readhead can be self-calibrated or reset to factory settings.

Position offset (encoder zero position)

The position offset is maped to registers 0x00, 0x01, 0x02, 0x03 of bank 0 in a big-endian format. The user must first write separate bytes of a new position offset in count values to these addresses. Afterwards, the user can read them to verify that the write operation is correct. At this point, the new position offset is not yet active. To validate it, the user must first unlock the command register by writing the KEY. The next register access must be a write of the Command to store the programmed data in non-volatile memory.

KEY: Value 0xCD at address 0x48
Command to store programmed data in non-volatile memory: ASCII ‘c’ (0x63) at address 0x49

> Programming of position offset larger than encoder resolution or smaller than zero is discarded.

Multiturn counter

Multiturn counter preset is only available in Multiturn version of Orbis. It is mapped to registers 0x04, 0x05, 0x06, 0x07 of bank 0 in big-endian format. The user must first write individual bytes of a new multiturn counter to these addresses. Then they can be read to verify the correct write operation. At this point, the new multiturn counter is not yet active. To validate it, the user must first unlock the command register by writing the KEY. The next register access must be a write of the Command to validate the value of the multiturn counter.

KEY: Value 0xCD at address 0x48
Command to validate the multiturn counter: ASCII ‘m’ (0x6D) at address 0x49

> Programming a multiturn counter greater than 65535 (unsigned) is discarded.

Self-calibration

The Orbis Self-calibration feature is suitable after mounting the readhead. It improves the accuracy of the encoder, which is dependent on the installation precision. User must first unlock the command register by writing the KEY (0xCD) to the Key register (address 0x48). The next register access must be a write of the SelfCal command (0x41) to the Command register (address 0x49) to start the self-calibration. During the process, no communication is possible via the BiSS interface; the encoder does not respond to incoming clock cycles. The completion of the process is indicated by fast flashing LED for 3 seconds. If the self-calibration was successful, LED flashes green, otherwise it flashes red. The BiSS interface is then active again. The status of the self-calibration can be read from a register 0x50. It consists of a two-bit counter and two status bits. The counter is incremented after the end of each self-calibration. Th error bits indicate the success or the reasons for failure.

Before the self-calibration process, the status should be read from register 0x50. The controller must remember the current self-calibration counter (bits 1:0). After the self-calibration command is sent, the user must observe LED to determine the completion of the process. If LED is not visible, the readhead should be polled via the BiSS interface until communication with the readhead is re-established. Or wait for 10 seconds, which is the longest possible time for completion. After that, the self-calibration status register should be read again. When the self-calibration counter has increased by 1 (compared to the previously read value), the self-calibration has been completed. If the self-calibration was successful, both status bits (b3, b2) are zero.

Rotation speed during self-calibration can be up to 600 RPM and may be uneven. The direction of rotation is not important.
At least one complete rotation during 10 s after sending the command is recommended. The self-calibration must be started when no error is present (green LED)

Self-calibration status register at address 0x52:

Bit	Meaning
b7 - b4	Reserved
b3	Calculated parameters out of range. Mechanical installation is not inside tolerances.
b2	Timeout. Encoder ring did not make a complete turn during 10 seconds.
b1	Counter bit 1
b0	Counter bit 0

KEY: value 0xCD to address 0x48
Command for starting self-calibration procedure: ASCII 'A' (0x41) to address 0x49.

Reset to factory settings

Resetting to factory defaults resets all programmed parameters to default values. The user must first unlock the command register by writing KEY. The next register access must be a write of the command to reset readhead to factory defaults.

KEY: Value 0xCD at address 0x48
Command to reset readhead to factory settings: ASCII 'r' (0x72) at address 0x49

Write protection

Write protection can be used to disable write access to any writable register in the Orbis memory map, except the Bank Select register. It is mapped to register 0x2E of bank 0, and its default value is 0x5A. To lock write access, the user must write a value other than 0x5A. To confirm write protection, the user should also store it to non-volatile memory. The write protect byte can be read back and verified after power cycle. After that, write access to all registers except Bank Select is denied. All registers then behave like non-writable registers.

The whole process is shown below.

WRITE PROTECT: Any value except 0x5A at address 0x2E
KEY: value 0xCD at address 0x48
Command for saving programmed data in non-volatile memory: ASCII ‘c’ (0x63) at address 0x49

> After write access has been disabled, the readhead can no longer be programmed. It can also not be reset to the factory settings. All registers can still be read.

User memory

The user memory, consisting of 4 kB RW registers, is mapped between banks 24 and 87. The user must first write the desired data into these registers. The data must then be stored in non-volatile memory. To do this, the user must first unlock the command register by writing the KEY. The next register access must be a write of the Command to save user data to non-volatile memory. The user memory banks also support sequential write access. It is possible to write multiple sequential registers in one access. For a detailed description of sequential write access, refer to the iC-Haus documentation.

KEY: Value 0xCD at address 0x48
Command for saving user data to a non-volatile memory: ASCII ‘u’ (0x75) to address 0x49

> User memory is no longer writable if write access is locked by the user.

Additional BiSS-C register access documentation

Documentation provided by iC-Haus describes BiSS-C register access in details:

- **BiSS Protocol Description**,
- **BiSS EDS Common Part**,
- **BiSS Standard Encoder Profile (BP3)**,
- **BiSS register access details 1**,
- **BiSS register access details 2**.

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Document issues

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