E201-9S
Decoding the BiSS information

The E201-9S interrogates a BiSS C encoder and allows data to be read by a PC with simple ASCII commands via a USB connection and a virtual COM port. The features of the BiSS data transmission and the details of the data packets are described in this document.

E201-9S supports unidirectional communication for absolute SSI and BiSS C encoders (without register access).

Related products

AksIM-2 & **AksIM-4** Rotary Absolute Magnetic Encoders

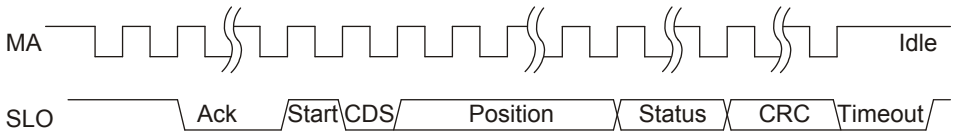
Artos Rotary Absolute Magnetic Encoder

LA11 Linear Absolute Magnetic Encoder

Orbis Rotary Absolute Magnetic Encoder

OnAxis Housed Absolute Rotary Magnetic Encoders

BiSS C (unidirectional) timing diagram



MA line is idle high. Communication is initiated with first falling edge.
The encoder responds by setting SLO low on the second rising edge at MA.
When the encoder is ready for the next request cycle, it indicates this to the master by setting SLO high. The absolute position and CRC data are in binary format and are sent with the MSB first.

Reading the encoder is started by sending the ASCII character “4” to the E201-9S interface. No CR character is required after the command.

The E201-9S returns a 16-character hexadecimal string + CR with 64 SLO bits, synchronized with 64 clocks MA.

Available in E201 interface version 1.16 (and later).

The data packet (with position, status and CRC) starts directly after the “010” sequence (ACK, Start, CDS).

If the sequence ACK is too long and the data packet falls out of the 64-bit word read by the E201-9S, the clock frequency of MA must be reduced.

Since the E201-9S does not make the line-delay compensation, it is possible that at some setting of MA clock frequency, the readout data will not be stable and produce CRC errors. In this case, select a different MA clock setting.

For the MA clock setting, see the “Mn” command in document E201D01, available at **RLS Media Center**.

Recommended clock frequencies for Renishaw Resolute encoders are 280 kHz and 560 kHz.

Example 1

Encoder used in example 1:

Type: Linear absolute encoder, BiSS output
Resolution: 0.05 µm
Position length: 32 bits
Status length: 2 bits (active low)
CRC length: 6 bits, polynomial $x^6 + x^1 + 1$ (Represented also as 0x43), inverted

Example of the response to the "4" command: **c0040030320ffac0** (hex)

Response																**Format**
C	0	0	4	0	0	3	0	3	2	0	F	F	A	C	0	**Hex**
1100	0000	0000	0100	0000	0000	0011	0000	0011	0010	0000	1111	1111	1010	1100	0000	**Binary**

Decoding the response into Position, Status and CRC:

First two bits are always "1"																
1100	0000	0000	0100	0000	0000	0011	0000	0011	0010	0000	1111	1111	1010	1100	0000	

Next "0" bits are the ACK bits. Number of ACK bits depends on encoder's latency and BiSS frequency.																
11**00**	**0000**	**0000**	**0**100	0000	0000	0011	0000	0011	0010	0000	1111	1111	1010	1100	0000	**ACK**

Start bit is always "1"																
1100	0000	0000	0**1**00	0000	0000	0011	0000	0011	0010	0000	1111	1111	1010	1100	0000	**Start Bit**

CDS bit is always "0"																
1100	0000	0000	010**0**	0000	0000	0011	0000	0011	0010	0000	1111	1111	1010	1100	0000	**CDS**

32 bits of POSITION = 0x00181907 = 1579271 counts																
1100	0000	0000	010**0**	**0000**	**0000**	**0011**	**0000**	**0011**	**0010**	**0000**	**111**1	1111	1010	1100	0000	**POSITION**

2 STATUS bits = 0x03																
1100	0000	0000	0100	0000	0000	0011	0000	0011	0010	0000	111**1**	**1**111	1010	1100	0000	**STATUS**

6 CRC bits = 0x3D																
1100	0000	0000	0100	0000	0000	0011	0000	0011	0010	0000	1111	1**111**	**101**0	1100	0000	**CRC**

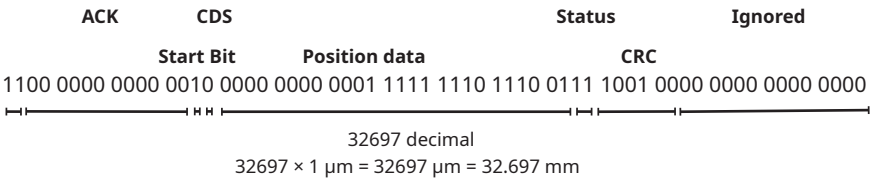
Ignored bits																
1100	0000	0000	0100	0000	0000	0011	0000	0011	0010	0000	1111	1111	101**0**	**1100**	**0000**	**Ignored**

Calculated encoder position = 1579271 counts × 0.05 µm = 78963.55 µm = 78.96355 mm
The status bits are 11. Since they are active low, the encoder operation is correct (no error, no warning).

Example 2

Encoder used in example 2:
Type: Linear absolute encoder, BiSS output
Resolution: 1 µm
Position length: 26 bits
Status length: 2 bits (active low)
CRC length: 6 bits, polynomial $x^6 + x^1 + 1$ (Represented also as 0x43), inverted

Response to the “4” command: **c002001fee790000** (hex) is decoded in binary as:



For CRC calculation example, refer to the document CRCD01, available at **RLS Media Center**.

Recommended literature:

- Painless guide to CRC error detection algorithm; Ross N. Williams.
- Cyclic Redundancy Code (CRC) Polynomial Selection For Embedded Networks; P. Koopman, T. Chakravarty
- Data sheet L-9709-9005 BiSS C-mode (undirectional) for Resolute encoders: http://www.renishaw.com/en/

Example 3

Encoder used in example 3:
Type: Rotary absolute multiturn encoder, BiSS output
Resolution: 19 bits
Multiturn resolution: 16 bits
Status length: 2 bits (active low)
CRC length: 6 bits, polynomial $x^6 + x^1 + 1$ (Represented also as 0x43), inverted

Example of the response to the "4" command: **c0010000c3298dc0** (hex).

Response																**Format**
C	0	0	1	0	0	0	0	C	3	2	9	8	D	C	0	**Hex**
1100	0000	0000	0001	0000	0000	0000	0000	1100	0011	0010	1001	1000	1101	1100	0000	**Binary**

Decoding the response into Position, Status and CRC:

First two bits are always "1"																
1100	0000	0000	0001	0000	0000	0000	0000	1100	0011	0010	1001	1000	1101	1100	0000	

Next "0" bits are the ACK bits. Number of ACK bits depends on encoder's latency and BiSS frequency.																
11**00**	**0000**	**0000**	**000**1	0000	0000	0000	0000	1100	0011	0010	1001	1000	1101	1100	0000	**ACK**

Start bit is always "1"																
1100	0000	0000	000**1**	0000	0000	0000	0000	1100	0011	0010	1001	1000	1101	1100	0000	**Start Bit**

CDS bit is always "0"																
1100	0000	0000	0001	**0**000	0000	0000	0000	1100	0011	0010	1001	1000	1101	1100	0000	**CDS**

16 bits of of MULTITURN = 0x1 = 1 count																
1100	0000	0000	0001	0**000**	**0000**	**0000**	**0000**	**1**100	0011	0010	1001	1000	1101	1100	0000	**POSITION**

19 bits of SINGLETURN POSITION = 275096 counts																
1100	0000	0000	0001	0000	0000	0000	0000	1**100**	**0011**	**0010**	**1001**	**1000**	1101	1100	0000	**SINGLETURN POSITION**

2 STATUS bits = 0x03																
1100	0000	0000	0001	0000	0000	0000	0000	1100	0011	0010	1001	1000	**11**01	1100	0000	**STATUS**

6 CRC bits = 0x1C																
1100	0000	0000	0001	0000	0000	0000	0000	1100	0011	0010	1001	1000	11**01**	**1100**	0000	**CRC**

Ignored bits																
1100	0000	0000	0001	0000	0000	0000	0000	1100	0011	0010	1001	1000	1101	1100	**0000**	**Ignored**

Calculated multiturn position = 1 count = 1

Calculated singleturn position = $\frac{275096 \text{ counts}}{2^{19}} \times 360 = 188.8934°$

The status bits are 11. Since they are active low, the encoder operation is correct (no error, no warning).

Example 4

Encoder used in example 4:
Type: Rotary absolute singleturn encoder, BiSS output
Resolution: 19 bits
Status length: 2 bits (active low)
CRC length: 6 bits, polynomial $x^6 + x^1 + 1$ (Represented also as 0x43), inverted

Example of the response to the "4" command: **c0014328ff300000** (hex).

Response																**Format**
C	0	0	1	4	3	2	8	F	F	3	0	0	0	0	0	**Hex**
1100	0000	0000	0001	0100	0011	0010	1000	1111	1111	0011	0000	0000	0000	0000	0000	**Binary**

Decoding the response into Position, Status and CRC:

First two bits are always "1"																
1100	0000	0000	0001	0100	0011	0010	1000	1111	1111	0011	0000	0000	0000	0000	0000	

Next "0" bits are the ACK bits. Number of ACK bits depends on encoder's latency and BiSS frequency.																
11**00**	**0000**	**0000**	**000**1	0100	0011	0010	1000	1111	1111	0011	0000	0000	0000	0000	0000	**ACK**

Start bit is always "1"																
1100	0000	0000	000**1**	0100	0011	0010	1000	1111	1111	0011	0000	0000	0000	0000	0000	**Start Bit**

CDS bit is always "0"																
1100	0000	0000	0001	**0**100	0011	0010	1000	1111	1111	0011	0000	0000	0000	0000	0000	**CDS**

19 bits of POSITION = 275087 counts																
1100	0000	0000	0001	0**100**	**0011**	**0010**	**1000**	**1111**	1111	0011	0000	0000	0000	0000	0000	**POSITION**

2 STATUS bits = 0x03																
1100	0000	0000	0001	0100	0011	0010	1000	1111	**11**11	0011	0000	0000	0000	0000	0000	**STATUS**

6 CRC bits = 0x33																
1100	0000	0000	0001	0100	0011	0010	1000	1111	11**11**	**0011**	0000	0000	0000	0000	0000	**CRC**

Ignored bits																
1100	0000	0000	0001	0100	0011	0010	1000	1111	1111	0011	**0000**	**0000**	**0000**	**0000**	**0000**	**Ignored**

$$\text{Calculated position} = \frac{275087 \text{ counts}}{2^{19}} \times 360 = 188.8872°$$

The status bits are 11. Since they are active low, the encoder operation is correct (no error, no warning).

Head office

RLS Merilna tehnika d. o. o.

Poslovna cona Žeje pri Komendi
Pod vrbami 2
SI-1218 Komenda
Slovenia

T +386 1 5272100
E mail@rls.si

www.rls.si

Global support

Visit our **website** to contact your nearest sales representative.

Document issues

Issue	Date	Page	Description
1	24. 8. 2015	-	New document
2	9. 2. 2017	1	BiSS C timing diagram amended
		3	6-bit CRC calculation description amended
3	29. 9. 2023	-	New design
		3 - 6	Examples amended