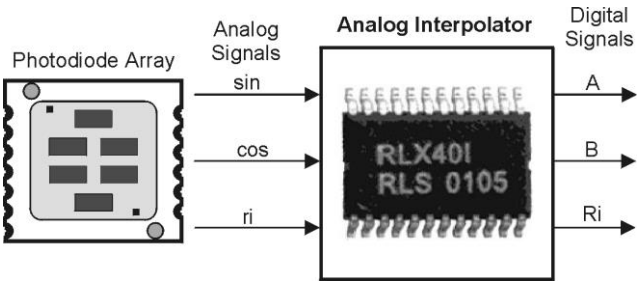
RLX40i

ANALOG INTERPOLATOR IC

RLX40i is not recommended for new designs. For more information please contact your local sales representative.

Features

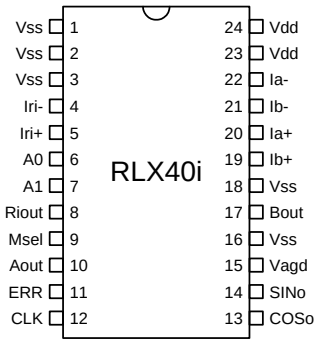
- Interpolation by 1, 2, 3, 4, 5, 8, 10
- Direct couplining of photodiode array
- Single power supply
- Low power
- High speed
- Short circuit proof
- Extended temperature range
- SMD package TSSOP24



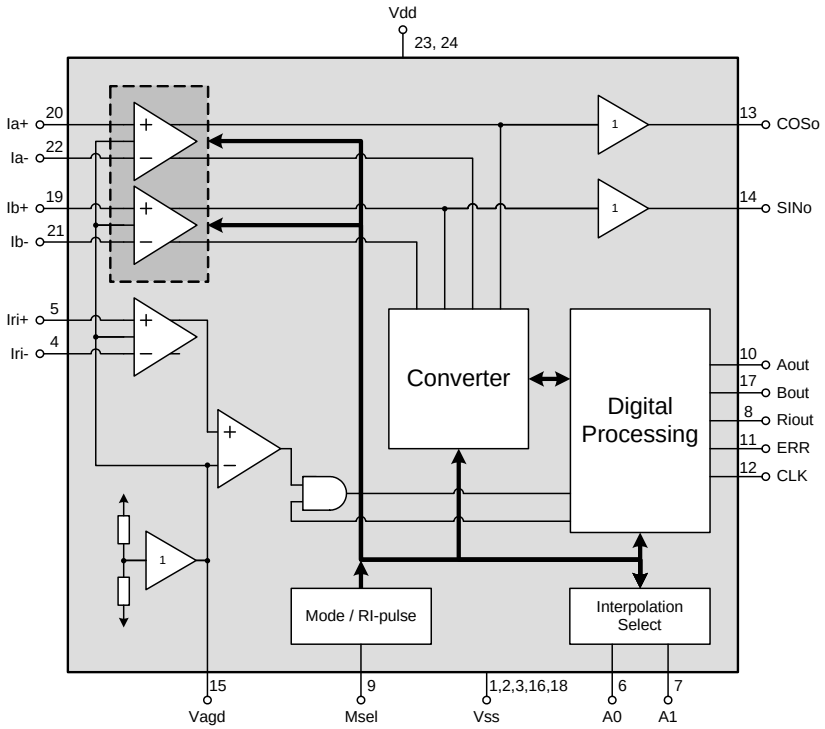
General description

The **RLX40i** is a monolithic integrated circuit which converts the input sine / cosine signals as well as the analog reference signal into digital signals with adjustable subdividing factor (1, 2, 3, 4, 5, 8, 10).
The monolithic converter produces two orthogonal digital incremental output signals **Aout** and **Bout**.
The reference (**Riout**) pulse width is selectable between 90º and 180º electrically.

Pin Assignment



Functional block diagram



Pin Description

Pin	Pin Name	Description	Comments
1	Vss	Negative Digital Supply Voltage	
2	Vss	Substrate Vss	
3	Vss	Negative Analog Supply Voltage	
4	Iri-	Ri inverted Input	Analog Input. Cin=7pf_typ
5	Iri+	Ri nonivnerted Input	Analog Input, Cin=7pf_typ
6	A_0	Interpolation factor select Input	Analog Input - internal pull up 100k
7	A_1	Interpolation factor select Input	Analog Input - internal pull up 100k
8	Riout	Output Ri	±4mA Output buffer
9	Msel	Input Channels mode Select	Analog Input - internal pull up 100k
10	Aout	Output A	±4mA Output buffer
11	ERR	Error signal Output	±2mA Output buffer
12	CLK	Error Clock Input	Digital Input - internal pull up 100k
13	COSo	Channel A Monitoring	Analog output – capacitive loading only
14	SINo	Channel B Monitoring	Analog output – capacitive loading only
15	Vagd	Ground – Buffered Mid, Supply	
16	Vss	Digital Substrate ring	
17	Bout	Output B	±4mA Output buffer
18	Vss	Analog Substrate PAD	bonding to external VSS is recomended
19	Ib+	B noninverted input	Analog Input - Sinus signal, Cin=7pf_typ
20	Ia+	A noninverted input	Analog Input – Cosine signal, Cin=7pf_typ
21	Ib-	B inverted input	Analog Input – inv. Sinus signal, Cin=7pf_typ
22	Ia-	A inverted input	Analog Input – inv. Cosine signal, Cin=7pf_typ
23	Vdd	Positive Digital Supply	
24	Vdd	Positive Analog Supply	

Electrical Characteristic

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	NOTE
DC Supply Voltage	Vdd	-0.3 V	7.0 V	
Input Pin Voltage	Vin	-0.3 V	Vdd + 0.3 V	
Input Current on any Pin	Iin	-100 mA	100 mA	25 °C
Operating temperature	To	-40 °C	+125 °C	
Storage Temperature	Tstg	-65 °C	150 °C	
Soldering Temperature	Tsol		260 °C	
Soldering Time			10 sec	1)
Humidity Non-condensing		5 %	85 %	
Electrostatic Discharge		2000 V		2)

1) 260 °C for 10 sec (reflow and wave soldering)
2) HBM: R = 1.5 kΩ, C = 100 pF

Working Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	NOTE
Power Supply Voltage	Vdd	4.0 V		5.5 V	
Supply Voltage Waviness	V_{AC}			50 mVpp	
Power Supply Current	Idd		5 mA	8mA	1)
Input current	Ia, Ib	2 µA	8 µA	18 µA	
Input current	Iri	1 µA	4 µA	9 µA	
Input impedance	Zin	60kΩ	80kΩ / 7pF	110kΩ / 10pF	
Input voltage - peak (single ended)	Va, Vb	0,4 V	0,8 V	1,2 V	
Input voltage - peak (differential)	Va, Vb	0,2 V	0,4 V	0,6 V	
Input frequency sine/cosine	fin			500 kHz	
Input CLK frequency	f_{CLK}			20 MHz	

1) 10µAp input, 100kHz analog inputs, 50pF load on signal current outputs and inputs, normal mode of operation, IP=5. Max. values are for IP=10.

Electrical Specifications

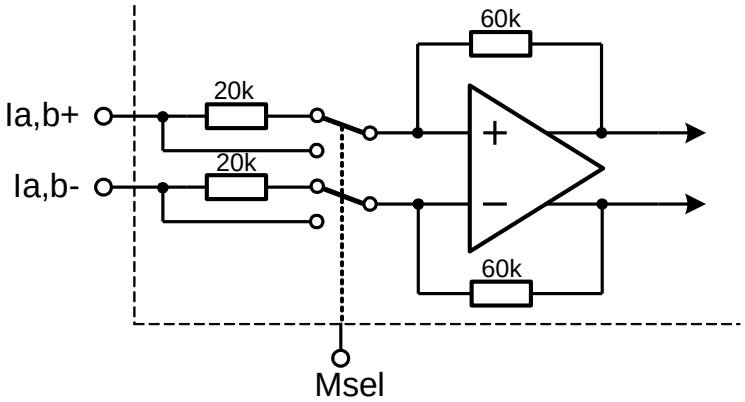
Selections

A1	A0	INTERPOLATION
Vss	Vss	1
Vss	NC	2
Vagd	Vagd	3
Vagd	NC	4
NC	NC	5 (default)
NC	Vagd	8
NC	Vss	10

NC - pin not necessary to be connected – internal pull up

Msel	Signal Mode	Index Duration (Riout)
Vss	Current Inputs	A&B tracks (90º)
NC	Voltage Inputs – set as default	A&B tracks (90º)
Vagd	Current Inputs	A track positive (180º)

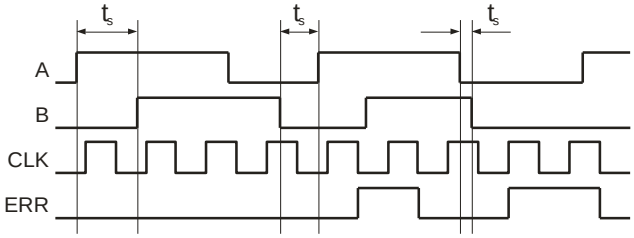
Input amplifier



The default gain is 3 for differential **Voltage inputs** – default setting.

To set any other gain, the **Current inputs** needs to be select. The voltage signals should be connect via appropriate resistors.

CLK - ERROR Timing



Error is detected when less than two fronts of **CLK** signal are inside **A**, **B** signals separation time (t_s). **ERR** signal appears at second next **CLK** front and lasts for one **CLK** period.

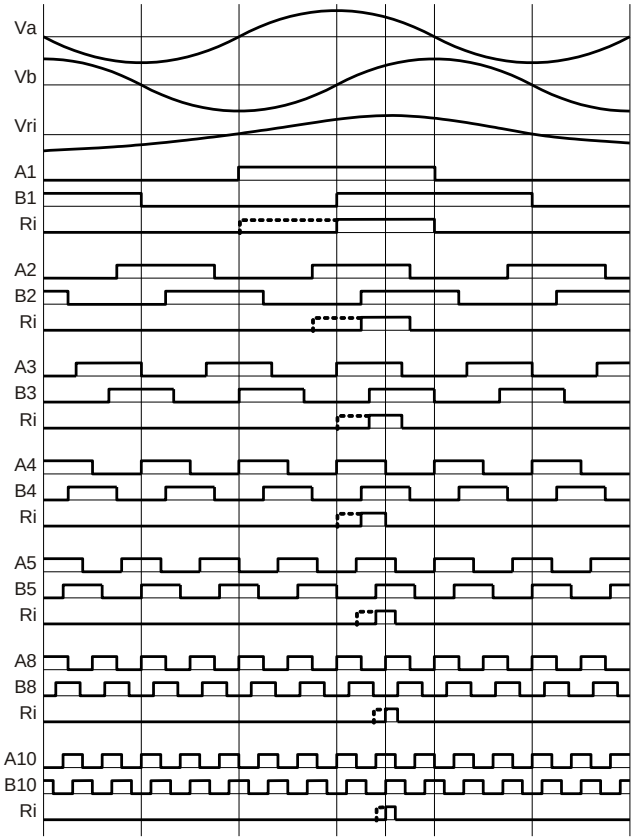
If there is no **CLK** front inside **A**, **B** signals separation time (t_s), **ERR** signal appears at second next CLK front and lasts for one and a half **CLK** period.

CLK frequency

$f_{CLK}= 4*f_{in}*FD/K$

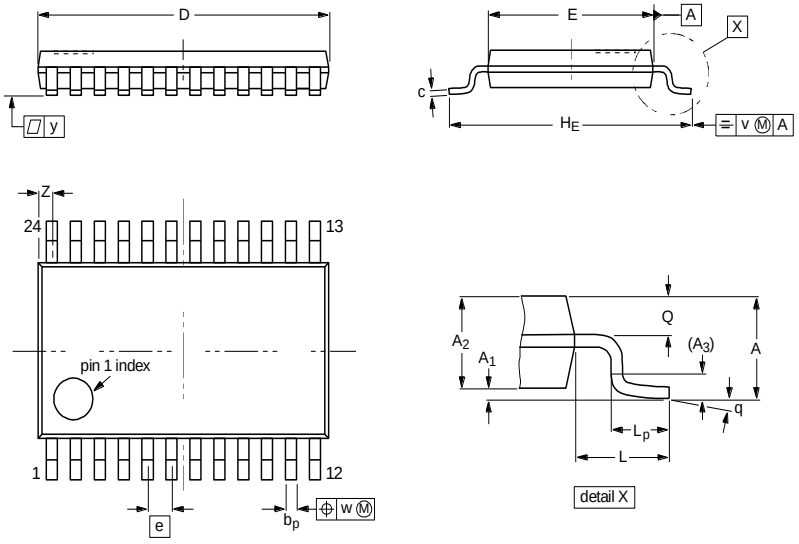
FD	division factor
f_{in}	analog input frequency
K<1	depends on analog input signals (amplitude, offsets, phase, high harmonics)

Typical Waveforms



* - ***Msel*** *use to select index pulse duration (equal to A track – 180 deg or A/B overlap – 90 deg)*

Physical dimensions TSSOP-24



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	q
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

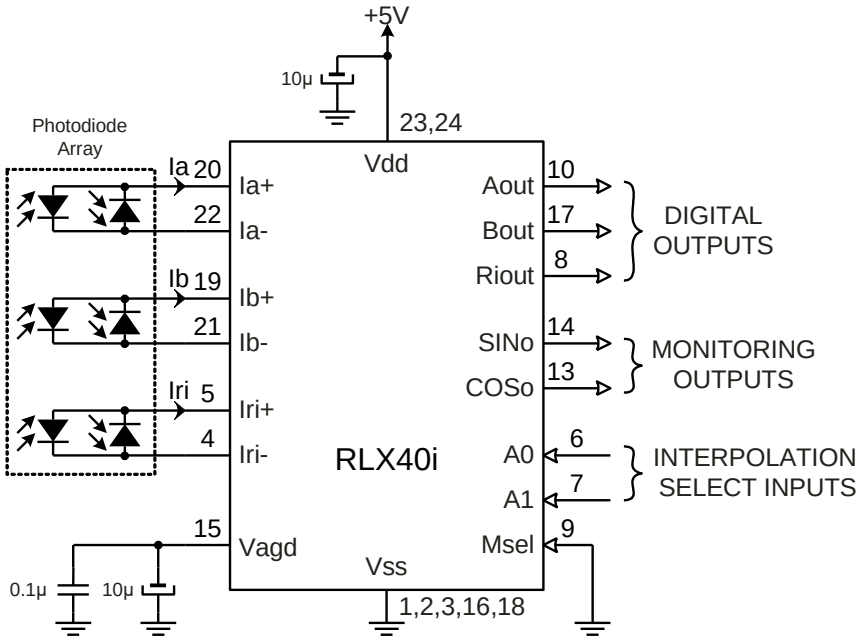
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

RLS merilna tehnika d.o.o.
Poslovna cona Žeje pri Komendi
Pod vrbami 2
SI-1218 Komenda, Slovenia

www.rls.si
Tel: +386 1 5272 100
Fax: +386 1 5272 129

Typical applications

1. Differential Current Inputs



2. Single ended inverted Voltage Inputs